AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

Claims 1-42 (canceled)

43. (currently amended) A chip structure comprising:

a silicon substrate;

a resistor in said silicon substrate, wherein said resistor comprises silicon with a dopant;

a MOS device comprising a portion in said silicon substrate;

a metallization structure over said silicon substrate, wherein said metallization structure comprises a first metal layer and a second metal layer over said first metal layer;

a first dielectric layer between said first and second metal layers;

a passivation layer over said metallization structure and over said first dielectric layer, wherein a first opening in said passivation layer is over a first contact point of a first metal interconnect of said metallization structure, and said first contact point is at a bottom of said first opening, and wherein a second opening in said passivation layer is over a second contact point of a second metal interconnect of said metallization structure, and said second contact point is at a bottom of said second opening, wherein a gap is between said first and second metal interconnects, wherein said first contact point is connected to said resistor ~~contact points~~, wherein said passivation layer comprises an insulating nitride layer; and

a circuit trace over said passivation layer and on said first and second contact points, wherein said first contact point is connected to said second contact point through said circuit trace~~, wherein said circuit trace is connected to said resistor through said first opening~~.

44. (previously presented) The chip structure as claimed in claim 43, wherein said dopant comprises boron.

45. (previously presented) The chip structure as claimed in claim 43, wherein said dopant comprises phosphorous.

46. (previously presented) The chip structure as claimed in claim 43, wherein said dopant comprises arsenic.

47. (previously presented) The chip structure as claimed in claim 43, wherein said dopant comprises gallium.

48. (previously presented) The chip structure as claimed in claim 43 further comprising a polymer layer on said passivation layer, wherein said circuit trace is further on said polymer layer.

49. (previously presented) The chip structure as claimed in claim 48, wherein said polymer layer comprises polyimide (PI).

50. (previously presented) The chip structure as claimed in claim 48, wherein said polymer layer comprises benzocyclobutene (BCB).

51. (previously presented) The chip structure as claimed in claim 43 further comprising a polymer layer on said circuit trace and over said passivation layer.

52. (previously presented) The chip structure as claimed in claim 51, wherein said polymer layer comprises polyimide (PI).

53. (previously presented) The chip structure as claimed in claim 51, wherein said polymer layer comprises benzocyclobutene (BCB).

54. (previously presented) The chip structure as claimed in claim 43 further comprising an inductor over said passivation layer.

55. (previously presented) The chip structure as claimed in claim 54, wherein said inductor comprises a copper layer.

56. (previously presented) The chip structure as claimed in claim 54, wherein said inductor comprises a gold layer.

57. (previously presented) The chip structure as claimed in claim 54, wherein said inductor comprises a titanium-containing layer and a copper layer over said titanium-containing layer.

58. (previously presented) The chip structure as claimed in claim 57, wherein said titanium-containing layer comprises a titanium-tungsten alloy.

59. (previously presented) The chip structure as claimed in claim 43 further comprising a capacitor over said silicon substrate, wherein said capacitor comprises a first electrode over said silicon substrate, wherein a third opening in said passivation layer is over said first electrode, a second dielectric layer on said first electrode and in said third opening, and a second electrode on said second dielectric layer and over said first electrode.

60. (previously presented) The chip structure as claimed in claim 59, wherein said second electrode comprises a gold layer.

61. (previously presented) The chip structure as claimed in claim 60, wherein said second electrode further comprises a titanium-containing layer under said gold layer.

62. (previously presented) The chip structure as claimed in claim 59, wherein said second electrode comprises a copper layer.

63. (previously presented) The chip structure as claimed in claim 59, wherein said second electrode comprises a copper layer and a nickel layer over said copper layer.

64. (currently amended) A chip structure comprising:

a silicon substrate;

a resistor in said silicon substrate, wherein said resistor comprises silicon with a dopant;

a MOS device comprising a portion in said silicon substrate;

a metallization structure over said silicon substrate, wherein said metallization structure comprises a first metal layer and a second metal layer over said first metal layer;

a dielectric layer between said first and second metal layers;

a passivation layer over said metallization structure and over said dielectric layer, wherein a first opening in said passivation layer is over a first contact point of a first metal interconnect of said metallization structure, and said first contact point is at a bottom of said first opening, and wherein a second opening in said passivation layer is over a second contact point of a second metal interconnect of said metallization structure, and said second contact point is at a bottom of said second opening, wherein a gap is between said first and second metal interconnects, wherein said first contact point is connected to said resistor ~~contact points~~, wherein said passivation layer comprises an insulating nitride layer; and

a circuit trace over said passivation layer and on said first and second contact points, wherein said first contact point is connected to said second contact point through said circuit trace, ~~wherein said circuit trace is connected to said resistor through said first opening,~~ wherein said circuit trace comprises a titanium-containing layer and a gold layer over said titanium-containing layer.

65. (previously presented) The chip structure as claimed in claim 64, wherein said dopant comprises boron.

66. (previously presented) The chip structure as claimed in claim 64, wherein said dopant comprises phosphorous.

67. (previously presented) The chip structure as claimed in claim 64, wherein said dopant comprises arsenic.

68. (previously presented) The chip structure as claimed in claim 64, wherein said dopant comprises gallium.

69. (previously presented) The chip structure as claimed in claim 64 further comprising a polymer layer on said passivation layer, wherein said circuit trace is further on said polymer layer.

70. (previously presented) The chip structure as claimed in claim 69, wherein said polymer layer comprises polyimide (PI).

71. (previously presented) The chip structure as claimed in claim 69, wherein said polymer layer comprises benzocyclobutene (BCB).

72. (previously presented) The chip structure as claimed in claim 64 further comprising a polymer layer on said circuit trace and over said passivation layer.

73. (previously presented) The chip structure as claimed in claim 72, wherein said polymer layer comprises polyimide (PI).

74. (previously presented) The chip structure as claimed in claim 72, wherein said polymer layer comprises benzocyclobutene (BCB).

Claims 75-82 (canceled)

83. (previously presented) The chip structure as claimed in claim 64, wherein said titanium-containing layer comprises a titanium-tungsten alloy.

84. (previously presented) The chip structure as claimed in claim 64, wherein said metallization structure comprises aluminum.

Claims 85-88 (canceled)

89. (currently amended) A chip structure comprising:

a silicon substrate;

a resistor in said silicon substrate, wherein said resistor comprises silicon with a dopant;

a MOS device comprising a portion in said silicon substrate;

a metallization structure over said silicon substrate, wherein said metallization structure comprises a first metal layer and a second metal layer over said first metal layer;

a dielectric layer between said first and second metal layers;

a passivation layer over said metallization structure and over said dielectric layer, wherein a first opening in said passivation layer is over a first contact point of a first metal interconnect of said metallization structure, and said first contact point is at a bottom of said first opening, and wherein a second opening in said passivation layer is over a second contact point of a second metal interconnect of said metallization structure, and said second contact point is at a bottom of said second opening, wherein a gap is between said first and second metal interconnects, wherein said first contact point is connected to said resistor ~~contact points~~, wherein said passivation layer comprises an insulating nitride layer; and

a circuit trace over said passivation layer and on said first and second contact points, wherein said first contact point is connected to said second contact point through said circuit trace, ~~wherein said circuit trace is connected to said resistor through said first opening,~~ wherein said circuit trace comprises a copper layer.

90. (previously presented) The chip structure as claimed in claim 89, wherein said dopant comprises boron.

91. (previously presented) The chip structure as claimed in claim 89, wherein said dopant comprises phosphorous.

92. (previously presented) The chip structure as claimed in claim 89, wherein said dopant comprises arsenic.

93. (previously presented) The chip structure as claimed in claim 89, wherein said dopant comprises gallium.

94. (previously presented) The chip structure as claimed in claim 89 further comprising a polymer layer on said passivation layer, wherein said circuit trace is further on said polymer layer.

95. (previously presented) The chip structure as claimed in claim 94, wherein said polymer layer comprises polyimide (PI).

96. (previously presented) The chip structure as claimed in claim 94, wherein said polymer layer comprises benzocyclobutene (BCB).

97. (previously presented) The chip structure as claimed in claim 89 further comprising a polymer layer on said circuit trace and over said passivation layer.

98. (previously presented) The chip structure as claimed in claim 97, wherein said polymer layer comprises polyimide (PI).

99. (previously presented) The chip structure as claimed in claim 97, wherein said polymer layer comprises benzocyclobutene (BCB).

100. (previously presented) The chip structure as claimed in claim 89, wherein said circuit trace further comprises a nickel layer over said copper layer.

101. (previously presented) The chip structure as claimed in claim 89, wherein said circuit trace further comprises a gold layer over said copper layer.

102. (previously presented) The chip structure as claimed in claim 89, wherein said circuit trace further comprises a nickel layer over said copper layer, and a gold layer over said nickel layer.